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<u>L16</u> 11 and L15	24	<u>L16</u>
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<u>L15</u> park-gi\$.in.	112	<u>L15</u>
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<u>L14</u> 12 with 13 and L13	90	<u>L14</u>
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<u>L13</u> 12 and L12	99	<u>L13</u>
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<u>L12</u> 17 and L11	121	<u>L12</u>
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<u>L11</u> 11 with 13 with 14	258	<u>L11</u>
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<u>L10</u> L8	841	<u>L10</u>
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DB=USPT; PLUR=YES; OP=OR

<u>L9</u> L8	575	<u>L9</u>
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<u>L8</u> 16 and L7	841	<u>L8</u>
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<u>L7</u> 711/\$.ccls.	34845	<u>L7</u>
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<u>L6</u> 11 and 15 and 14	1465	<u>L6</u>
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<u>L5</u> 11 with 13	4037	<u>L5</u>
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<u>L4</u> miss	61093	<u>L4</u>
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<u>L3</u>	cach\$	166000	<u>L3</u>
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» Key

IEEE JNL IEEE Journal or Magazine

IET JNL IET Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IET CNF IET Conference Proceeding

IEEE STD IEEE Standard

- ☐ 1. **Thermal management of on-chip caches through power density minimization**
Ja Chun Ku; Ozdemir, S.; Memik, G.; Ismail, Y.;
[Microarchitecture, 2005. MICRO-38. Proceedings. 38th Annual IEEE/ACM International Symposium on](#)
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- ☐ 2. **Power monitors: a framework for system-level power estimation using heterogeneous power models**
Bansal, N.; Lahiri, K.; Raghunathan, A.; Chakradhar, S.T.;
[VLSI Design, 2005. 18th International Conference on](#)
3-7 Jan. 2005 Page(s):579 - 585
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- ☐ 3. **Combined circuit and architectural level variable supply-voltage scaling for low power**
Hai Li; Chen-Yong Cher; Roy, K.; Vijaykumar, T.N.;
[Very Large Scale Integration \(VLSI\) Systems, IEEE Transactions on](#)
Volume 13, Issue 5, May 2005 Page(s):564 - 576
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[Microarchitecture, 2003. MICRO-36. Proceedings. 36th Annual IEEE/ACM International Symposium on](#)
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- ☐ 5. **Cosimulation-based power estimation for system-on-chip design**
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- ☐ **6. A power-aware SWDR cell for reducing cache write power**
Yen-Jen Chang; Chia-Lin Yang; Feipei Lai;
[Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on](#)
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- ☐ **7. Quantitative analysis and optimization techniques for on-chip cache leakage power**
Nam Sung Kim; Blaauw, D.; Mudge, T.;
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- ☐ **8. Design and analysis of low-power cache using two-level filter scheme**
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- ☐ **9. Circuit and microarchitectural techniques for reducing cache leakage power**
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- ☐ **10. Leakage power optimization techniques for ultra deep sub-micron multi-level caches**
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- ☐ **11. Tag compression for low power in dynamically customizable embedded processors**
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- ☐ **12. Soft errors issues in low-power caches**
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- ☐ **13. Power protocol: reducing power dissipation on off-chip data buses**
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- ☐ **16. An energy efficient instruction set synthesis framework for low power embedded system designs**
Cheng, A.C.; Tyson, G.S.;
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Digital Object Identifier 10.1109/TC.2005.89
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- ☐ **17. A 2.2 W, 80 MHz superscalar RISC microprocessor**
Gerosa, G.; Gary, S.; Dietz, C.; Dac Pham; Hoover, K.; Alvarez, J.; Sanchez, H.; Ippolito, P.; Tai
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- ☐ **18. Power efficient resource scaling in partitioned architectures through dynamic heterogeneity**
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- ☐ **19. Tag skipping technique using WTS buffer for optimal low power cache design**
Akaaboune, A.; Botros, N.; Alghazo, J.;
[Memory Technology, Design and Testing, 2004. Records of the 2004 International Workshop on](#)

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- ☐ **20. Value-conscious cache: simple technique for reducing cache access power**
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- ☐ **21. Using complete machine simulation for software power estimation: the SoftWatt approach**
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- ☐ **22. Synthesis techniques for low-power hard real-time systems on variable voltage processors**
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- ☐ **23. Power analysis of embedded software: a first step towards software power minimization**
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- ☐ **24. Reducing power density through activity migration**
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[Low Power Electronics and Design, 2003. ISLPED '03. Proceedings of the 2003 International Symposium on](#)
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- ☐ **25. Avalanche: an environment for design space exploration and optimization of low-power embedded systems**
Henkel, J.; Yanbing Li;
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Volume 10, Issue 4, Aug. 2002 Page(s):454 - 468
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